IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A cache memory device comprising:

at least one cache memory storing copy data of a main memory, and

a bank control circuit, connected to said at least one cache memory, and capable of generating a plurality of control signals for access to said at least one cache memory, said bank control circuit receiving a signal indicative of cache capacity from outside the cache memory device and permitting at least one control signal selected out of said plurality of control signals to access said at least one cache memory, respectively, in accordance with said signal indicative of cache capacity.

Claim 2 (Original): The cache memory device according to claim 1, wherein said bank control circuit controls access to said at least one cache memory in such a manner that one accessing operation implements access to only one out of said at least one cache memory.

Claim 3 (Currently Amended): The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories, said cache memory device further comprising a power control circuit for controlling power supply to said plurality of cache memories connected to said bank control circuit based on said signal indicative of cache capacity,

said power control circuit only supplying [[a]] power to ~~only~~ the one or more cache memories accessed with said at least one control signal selected by said bank control circuit out of said plurality of cache memories.

Claim 4 (Currently Amended): The cache memory device according to claim 1, wherein a cache address indicating an address of said main memory and including a tag and an index is input to said cache memory device,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag [[in]] <u>of</u> said cache address,

said cache memory device further comprising:

a cache peripheral circuit for linking said index in said cache address input to said cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit is accessed, to data in said tag memory stored in said address indicated by said index, and for generating and outputting a copy back address,

a copy back method using said copy back address being employed as a writing method for said main memory.

Claim 5 (Currently Amended): The cache memory device according to claim 1, wherein a cache address indicating an address of said main memory and including a tag and an index is input to said cache memory device,

a bit position occupied by said tag and said index is fixed in said cache address, said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag [[in]] <u>of</u> said cache address,

said cache memory device further comprising:

a comparator for comparing said tag in said cache address input to said cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit is accessed, to data in said tag memory stored in said address indicated by said index in said cache address, and for detecting their coincidence/non-coincidence.

Claim 6 (Currently Amended): The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories,

a cache address indicating an address of said main memory and including a tag is input to said cache memory device,

a bit position occupied by said tag is fixed in said cache address,

said plurality of cache memories have respective tag memories for storing said tag [[in]] of said cache address, and

said respective tag memories store plural pieces of fixed data ~~peculiar~~ unique to said plurality of cache memories, respectively, each of said plural pieces of fixed data corresponding to a part of said tag.

Claim 7 (Original): The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories, and

said plurality of cache memories have the same memory capacity.

Claims 8-14 (Cancelled).

Claim 15 (Currently Amended): A bank control circuit controlling an access to a cache memory, comprising;

a decoder receiving first and second signals from outside a cache memory device in which said bank control circuit is located and outputting bank select signals such that one of the bank select signals is active in accordance with said first and second signals, wherein said first signal is indicative of a cache capacity used in the cache memory and said second signal is a part of an address supplied to the cache memory, and

signal output circuits provided correspondingly to the bank select signals, respectively, each signal output circuit receiving a control signal for accessing the cache memory and a corresponding bank select signal, and permitting the control signal to be output to the cache memory in response to an active state of said corresponding bank ~~control~~ select signal while inhibiting said control signal to be output to the cache memory in response to a non-active state of said corresponding bank ~~control~~ select signal.